APPENDIX

In the Specification:

Please replace the paragraph on page 13, line 19, as follows:

In the illustrated embodiment, the home agent 411 of the AXQ module 383 includes a variety of modules, such as a secondary transfer buffer (STB) 412, a victim rewrite buffer (VRB) 413, an invalidation tag identifiers (ITI) 414, en-direct-map [(EM)] (DM) 415, and one or more counters 416, all of which are described in more detail below. The request agent 420, in the illustrated embodiment, includes one or more counters 421. It should be appreciated that the components of the AXQ module 383 shown in Figure 4 are exemplary in nature and that in other embodiments fewer or additional components may be employed, depending on the implementation.

Please replace the paragraphs on page 15, line 20, through page 17, line 5, as follows:

The design verification module 440 of the home agent [420] 411 may adjust the number of STBs in use. Typically, tags associated with the STB 412 only apply to certain types of address transactions, specifically read-to-share and write-back transactions, where a read-to-share transaction is issued to obtain a shared copy of a cache line and a write-back transaction to write the cached line back to the memory. By adjusting the number of STBs 412 that are available for use, the design verification module 440 is more selective in the manner the transaction flow is restricted, as compared to adjusting the number of available working address transaction identifiers. By selectively restricting the transaction flow, the design verification module 440 of the home agent [420] 411 may exercise the system 10 in a manner (*e.g.*, by disrupting the natural flow of transactions) such that one or more design flaws may be more readily discoverable.

The design verification module 440 of the home agent [420] 411 may adjust the number of VRBs 413 in use. The function of the VRB 413 is generally related to shared entries in the directory cache [396] 430 that are victimized (*i.e.*, entries that need to be written back to home memory). The VRB 413 may thus restrict the number of outstanding entries currently written back to home memory at any given time, thereby exercising the system 10 in a manner that may reveal design flaws in the system 10.

Similarly, the design verification module 440 of the home agent [420] 411 may utilize the ITI 414 to adjust the number of invalidation tags that are available for slave broadcast of shared directory cache victimizations and normal writestream transactions. A writestream transaction may be utilized to write a copy of a cache line. By adjusting the number of available invalidation tags, the design verification module 440 of the home agent [420] 411 may exercise the system 10 in a manner to reveal one or more design flaws that otherwise may not have been so readily discoverable.

The design verification module 440 of the home agent [420] 411 may utilize the DM 415 to reduce the two-way set associative lock structure of the home agent [420] 411 to a one-way lock structure. For example, the lock structure may be reduced from 16 locks to 8 locks. The DM 415 thus may be used to limit the number of outstanding transactions that have obtained "locks," where obtaining a "lock" allows the transaction to complete in the rest of the system 10. In this manner, the design verification module 440 of the home agent [420] 411 is able to place the system 10 in a state where one or more errors may be more readily discovered.

Please replace the paragraph on page 20, line 22, through page 21, line 6, as follows:

As mentioned, a user may configure any number of a variety of the above-mentioned parameters in the system 10 to allow the system 10 to readily enter states that may have been difficult or rare to achieve during normal operations. Once the parameters in the system 10 are configured (at 520) in the desirable manner, the user may execute (at 553) one or more programs in the system 10. These executable programs, when running on the system 10, may reveal design flaws that may not have otherwise been exposed had the system 10 not been configured (at 520) in the desirable manner. In one embodiment, diagnostic programs (*i.e.*, as opposed to typical programs) may also be executed (at [520] 553) to reveal design flaws in the system 10.

In the Claims:

Please amend claims 11 as follows:

11. (Amended) The system of claim 7, wherein the second device comprises an anti-starvation logic to gain control of a bus, and wherein the second configuration comprises the second device employing the anti-starvation logic to access the bus during an interval the bus is not being asserted by the first device.

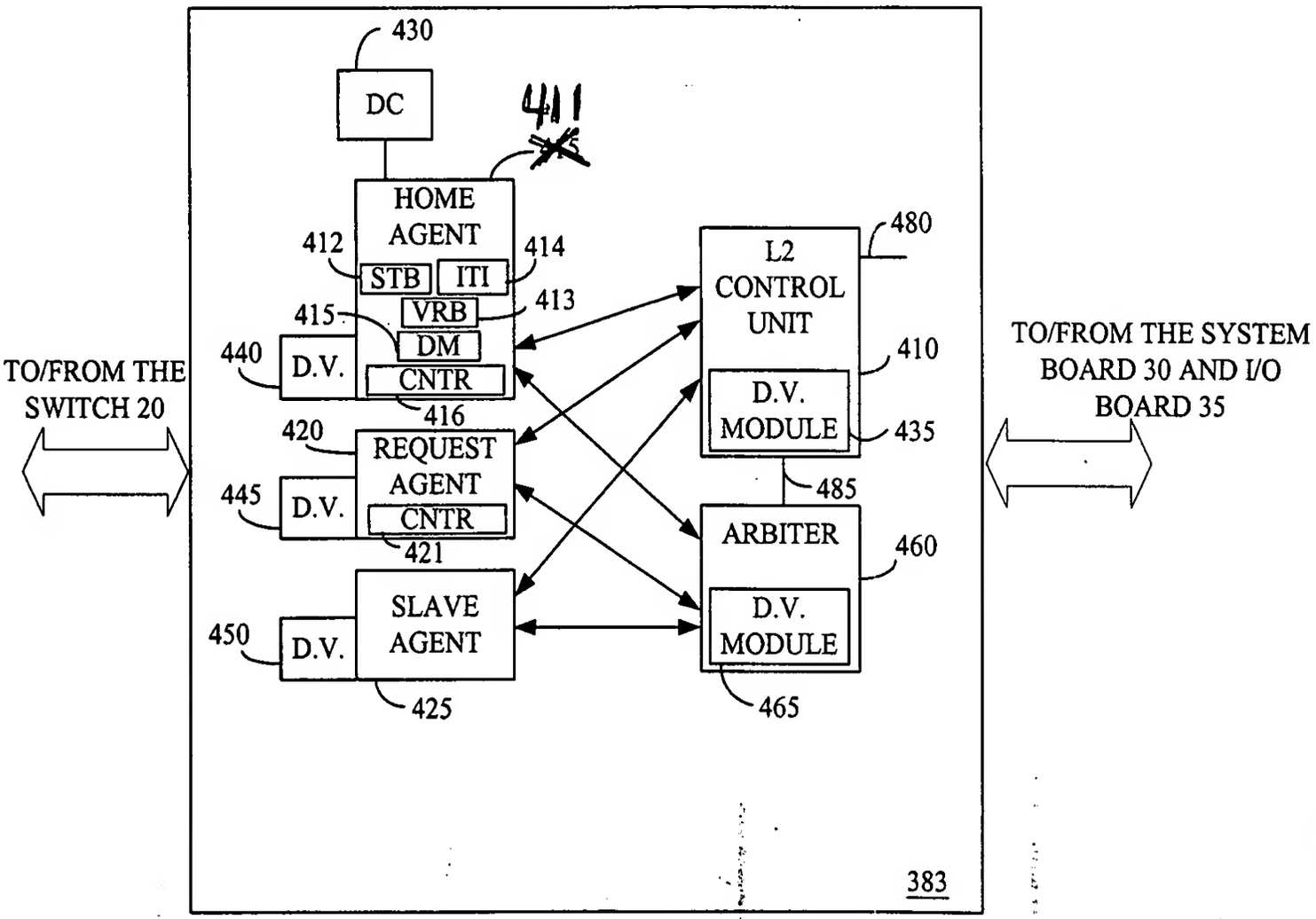

Figure 4